Current Mode Image Sensor With Improved Linearity and Fixed-Pattern Noise

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***Abstract*—Current mode active pixel sensors convert light intensity into an analog output current. A current mode image sensor enables simple implementation of focal plane algebraic functions but suffers from poor linearity and large fixed-patten noise. This paper analyzes the causes of the non-linearity of a current-mode image sensor including a theoretical derivation and numerical simulation. Previously reported linearity improvement methods are reviewed, while an architecture of a current mode image sensor with a voltage feedback loop between pixel output and the current conveyor for linearity enhancement is proposed. An image sensor array of 100 × 200 current mode pixels is fabricated in a 0.5 μm 2P3M standard CMOS processing technology. Experimental results illustrate a 45% improvement of the linearity of the proposed imager. Fixed pattern noise is reduced by 57.6% for the maximum readout current, which can be further reduced by another 51.5% after gain calibration. A signal to noise ratio of 49.6 dB is achieved.**

***Index Terms*—Current mode image sensor, fixed-pattern noise, linear response.**

I. Introduction

In the last decades, the use of image sensors has increased exponentially due to the growth of mobile devices. There are two image sensor design paradigms: CCD and CMOS image sensors. In 1968, a MOS pixel image sensor with integrated off-array amplifier was proposed [1]. However, it was not widely used at that time due to the limitations of MOS technology. Two years later in 1970, the CCD image sensor was invented at Bell Labs, which has dominated both the image sensor industry and academic research for almost 30 years. The market share of CCD and CMOS image sensors started to change in 1990s when the three transistor active pixel sensor (APS) topology was proposed [2]. Nowadays, APS has been accepted as a standard for state-of-the-art image sensors. Compared to a CCD imager, the technology for a CMOS sensor is less expensive, provides higher resolution, and has lower power consumption [3].

In recent years, on-chip image processing capabilities have become more and more significant considerations for both still image and video devices. CMOS image sensor arrays with integrated analog-to-digital converter (ADC) [4], focal plane processing [5]–[7] and on-chip memory [8] have been reported in the literature, realizing a camera-on-chip. The majority of CMOS image sensors work in the voltage domain, referring to the fact that the pixel output is a voltage and the subsequent processing is done in the voltage domain. Compared to voltage domain processing, current domain processing allows for simple implementation of focal plane algebraic functions, such as addition, subtraction and scaling. It is for this reason that current-mode imagers and processing have received increasing attention in the last decade from visual imagers [14]–[18], to X-ray imaging devices [19]–[21].

In active pixel sensors (APS), a photodiode is employed in each pixel to convert incident light intensity into an analog signal, which can be read out in terms of either current or voltage, depending on the readout circuit's operation mode. In voltage mode APS [2], the converted voltage is stored on the photodiode's parasitic capacitance and is read out through a source follower. On the other hand, the readout transistor in a current mode APS is biased in either the linear region or velocity saturation region generating a current proportional to the incident light intensity [9]–[13], [16]. The readout of a current mode APS can be a logarithmic [9], quadratic [10], [12], or linear [11], [13], [16] function of the incident light intensity. The current mode APS provides the potential of high speed readout, since the readout line is biased at a fixed voltage, delivering current instead of voltage for different light intensity levels, which requires no charging and discharging of the parasitic capacitance. This characteristic of current mode APS makes it well suitable for focal-plane processing such as motion detection, image compression, and polarization reconstruction [22].

Unfortunately, high power consumption, high noise level, and non-linearity have prevented current mode APS from being the technology of choice, despite its potential advantages. In current mode APS, the fixed pattern noise (FPN) is typically higher than that in the voltage mode APS [2]. Various methods have been reported to reduce the FPN. Paper [32] reported a calibration method using an in-pixel voltage ramp. Paper [33] proposed a on-chip calibration method using a two-step charge transfer. However, the implementation of the calibration is difficult due to the nonlinearity characteristic. Also, the additional processing complexity increases the power consumption and reduces the performance of the pixel, e.g. the fill factor. Other methods have been proposed in the literature to improve the performance of current mode APS. Paper [10] introduces an integrated column-level FPN suppression circuit which subtracts the offset current from the signal current. Paper [23] proposed to

Manuscript received May 30, 2013; revised September 01, 2013 and October 08, 2013; accepted October 19, 2013. Date of publication April 15, 2014; date of current version May 23, 2014. This paper was recommended by Associate Editor T. S. Gotarredona. *(Corresponding author: M. Zhang.)*

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Digital Object Identifier 10.1109/TCSI.2013.2295009

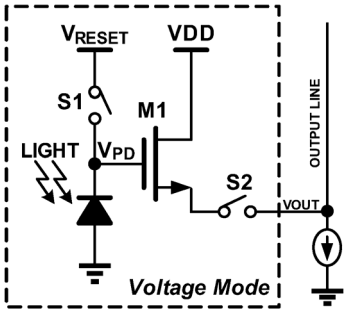


Fig. 1. Architecture of a standard 3-transistor voltage mode APS.

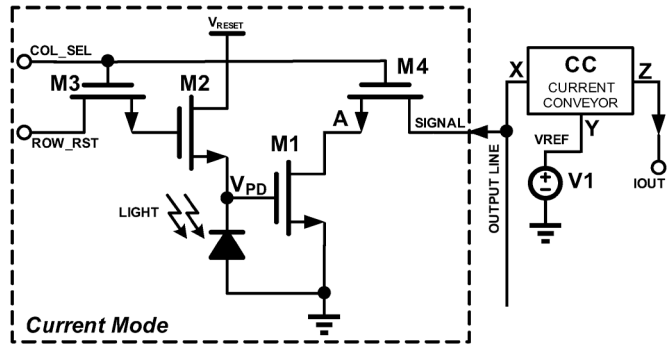


Fig. 2. Architecture of a standard current mode APS.

improve the spatial variation by reducing the transistor number within each pixel from three to two, therefore lowering the FPN resulting from the variation of the output transistors. Since current-mode difference double sampling [23] can be employed to further reduce the spatial variation, the noise performance of current mode APS has been improved considerably.

In this paper, we first analyze the cause of the non-linearity in current mode image sensors, as well as review the various methods for improving the linearity as discussed in the literature. Derivation and numerical analysis of the non-linearity are included. We propose a novel scheme to increase the linearity of the I-V transfer curve by introducing a feedback loop between the pixel and the current conveyor. An image sensor array consisting of 100×200 current mode pixels is fabricated in 0.5 μm processing technology. Experimental results illustrate an 45% improvement of the linearity of the proposed imager. A 57.6% reduction in fixed pattern noise and a signal to noise ratio of 49.6 dB is achieved, which can be further reduced by another 51.5% after a gain calibration.

The paper is organized as follows. An analysis and review of the linearity of a standard APS operating in the current mode is derived in Section II. The architecture of the pixel and an overview of the complete imaging system are proposed in Section III. Experimental results of the fabricated image sensor are presented in the following section. Section V concludes the overall work.

II. Review of Current Mode APS Design

A. Voltage Mode v.s. Current Mode APS Designs

The architecture of a standard 3-transistor voltage mode APS is illustrated in Fig. 1. The process starts with a reset phase during which the photodiode voltage V_{PD} is pulled up to V_{RESET} through switch S_1. The photodiode voltage V_{PD} is discharged proportionally to the light intensity and the integration time after the reset switch S_1 is opened. During the readout phase, the discharged photodiode voltage is transferred to the output line through a source follower M_1. Depending on the imager structure, the data bus may be shared by the whole pixel array for chip level readout, or by a pixel column for column level readout.

The architecture of a standard current mode APS is very similar to that of the voltage mode, as illustrated in Fig. 2. The sensing process starts with a reset phase controlled by a select switch M_3 during which the photodiode voltage V_{PD} is pulled up to a preset value V_{RESET} through switches M_2. Then, the integration phase begins right after M_2 opens which causes V_{PD} to drop proportionally to the light intensity and the integration time, similarly to the voltage mode pixel. The difference is the operation mode of the amplifier transistor M_1 which is now used as a transconductance amplifier within each pixel, converting V_{PD} to its drain current. The output current from the pixel is transferred to the current conveyor (CC) and mirrored out as an analog current representing the pixel readout value.

In the voltage mode APS, during the readout phase, the selected pixel must charge or discharge the readout line to the required output voltage through the in-pixel source follower. However, in current mode APS, the readout line is biased at a fixed voltage to deliver the current output for each pixel during readout phase. No charging/discharging of the parasitic capacitance is required, resulting in a faster readout process. In addition, in voltage mode APS, the dynamic range is affected by the reset voltage, while in current mode APS, there is no such strict constraint in the configuration of the reset voltage. A current mode image sensor can be designed in a low supply process without sacrificing the dynamic range. However, the linearity of a current mode APS is a serious bottleneck in the improving of the performance. In the following, we will focus on the origins of non-linearity in current mode image sensors.

B. Non-Linearities in the Current Mode Image Sensor

The nonlinearity characteristic in an active pixel sensor reduces the performance of the noise suppression circuit [10], since existing first-order FPN cancellation techniques assume linearity [16]. The nonlinearities also reduce the dynamic range and precision of the analog computation in current mode image sensors.

In each pixel, the readout transistor can be biased in two regions: linear (triode) region and saturation (active) region under velocity saturation. The linearity of $g_{m_{pxl}}$ can be improved by biasing the transistor in the proper region. In a standard current mode APS as shown in Fig. 2, a NMOS transistor, $M1$, is employed as the readout transistor. The photon integration voltage $qe-/C_{pxl}(V)$ set the value of V_{GS}. Taking velocity saturation into effect, the output current of readout transistor in the linear (triode) region can be expressed as in (1) [25].

$$I_{DS} = \frac{\mu_n C_{ox}}{2\left(1+\frac{V_{DS}}{E_C L}\right)} \frac{W}{L}\left[2(V_{GS}-V_{TH})V_{DS} - V_{DS}^2\right] \quad (1)$$

where E_C is the critical field indicating the onset of the saturation for the carrier's (electrons for NMOS and holes for PMOS) mobility. If the velocity saturation is not significant ($E_C L \gg V_{DS}$), (1) can be simplified to the well-known form

$$I_{DS} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right] \quad (2)$$

From (1), the value of $g_{m_{pxl}}$ while biasing in linear region can be expressed as

$$g_{m_{pxl-lin}} = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\mu_n C_{ox} V_{DS} E_C W}{V_{DS} + E_C L} \quad (3)$$

The nonlinearity of $g_{m_{pxl-lin}}$ mainly comes from the variation of V_{DS}, and the mismatch of W and L.

For transistors in the saturation (active) region, the output current of the readout transistor can be written as [31]

$$I_{DS} = \frac{\mu_n C_{ox} W\left[2(V_{GS} - V_{TH}) - V_{DSAT}\right]V_{DSAT}}{E_C L + V_{DSAT}} \quad (4)$$

where the V_{DSAT} can be expressed as

$$V_{DSAT} = \frac{E_C L(V_{GS} - V_{TH})}{E_C L + (V_{GS} - V_T)} \quad (5)$$

If the velocity saturation is not significant ($E_C L \gg V_{GS} - V_{TH}$), V_{DSAT} becomes $V_{GS} - V_{TH}$, and (4) can be simplified to the well-known form

$$I_{DS} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 \quad (6)$$

If the velocity is completely saturated ($E_C L \ll V_{GS} - V_{TH} < V_{DS}$), (4) reduces to (7) [24]

$$I_{DS} = \mu_{sat} C_{ox} W E_C (V_{GS} - V_{TH}) \quad (7)$$

Then the readout transistor's transconductance in saturation region under velocity saturation can be expressed as

$$g_{m_{pxl-sat}} = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{sat} C_{ox} W E_C, (E_C L \ll V_{DS}) \quad (8)$$

Thus the main nonlinearity of the transconductance in the saturation region comes from the mismatch of the width of the readout transistor ΔW, and the condition for onset of velocity saturation $E_C L \ll V_{DS}$.

Previous approaches to enhance the linearity of $g_{m_{pxl}}$ have been reported in literature. Papers [22], [23] proposed to improve the I-V curve by employing a large column-parallel switch with a smaller parasitic resistance. [13], [24] proposed improving the linearity by biasing the readout transistor in the velocity saturation region. However, all reported methods ignored the fact that the drain voltage V_{DS} plays an important role in the linearity of $g_{m_{pxl}}$ as shown in ((3), (8)).

In a current mode APS (Fig. 2), the drain voltage V_{DS} (node A) of the readout transistor M_1 is biased through the CC (node X) to a constant voltage V_{REF}, set by V_1 (node Y). With increasing resolution of image arrays, and decreasing feature size of the transistors, the effect of the voltage drop over the parasitic line resistance (from node X to node A), and thus variation of V_{DS} with the signal current can not be ignored.

In order to quantitatively evaluate this effect, a test bench as shown in Fig. 3 is set up to simulate the V_{DS} variation. Where

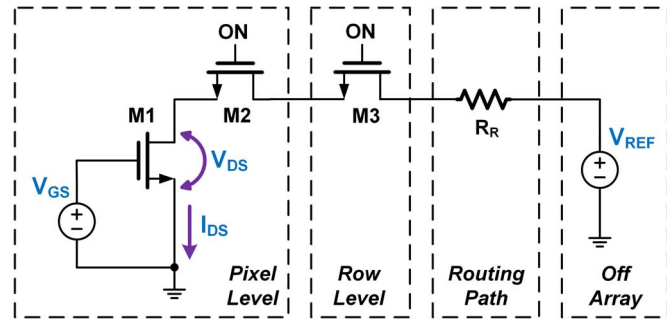


Fig. 3. Simulation testbench of the effect of parasitic resistance on the variation of V_{DS}.

$M2$ is the in-pixel select switch, $M3$ is the row level select switch, and R_R represents the parasitic resistance in the routing path. There are three main sources of the parasitic resistance:

1) On-resistance R_{M2} of the selection switch M_2 in each pixel;
2) On-resistance R_{M3} of the row selection switch M_3;
3) Parasitic resistance R_R of the routing from each pixel to the current conveyor.

The first two resistances R_{M2} and R_{M3} vary spatially from pixel to pixel, row to row due to transistor mismatches, and also vary for different signal levels. The parasitic resistance in the routing path R_R varies with the routing length from the pixel to the current conveyor. A numerical analysis of 0.5 μm process is done to investigate the variation of parasitic resistance. A NMOS switch with W/L = 0.9 μm/0.6 μm, has a simulated on-resistance from 5 kΩ to 15 kΩ depending on the terminals' voltage. The sheet resistance is 0.05 $\Omega/\square$ for the top metal layer. For a 500 × 500 pixel array composed of 10 μm × 10 μm pixels, if the top metal layer is used to transfer the pixel output current to the readout circuit, with a trace width of 0.9 μm, the approximate trace resistance is around 300 Ω.

A Monte-Carlo simulation is conducted to investigate the effect of the V_{DS} variation. Extracted parasitic resistances are employed. The simulation results given in Fig. 4 shows that V_{DS} variation is mainly introduced by the I-R drop along the signal path connecting the pixel and the current conveyor. For a pixel operating in the velocity saturation mode, 100 μA output current is expected when exposed to low light intensity. Thus, the total I-R drop is as large as 2 V which will lead to significant errors to the readout current. With further processing scaling, the parasitic resistance will become even larger because such process usually has larger sheet resistance for lower level metal interconnections.

C. Noise Analysis

The current readout of a pixel can be modeled as:

$$I_{readout} = G_{CC}\left[g_{m_{pxl}}\left(\frac{Q_{photon}}{C_{pxl}} + V_{DC_{pxl}}\right)\right] + I_{DC_{CC}} \quad (9)$$

where Q_{photon} is the photon-generated charges, G_{CC} and $g_{m_{pxl}}$ are the gain and transconductance of the current conveyor and the readout transistor, $V_{DC_{pxl}}$ is the DC offset of the the readout transistor, $I_{DC_{CC}}$ is the DC offset of the current conveyor, and C_{pxl} is the well capacity of the pixel. Assume the gain and transconductance in the current conveyor and

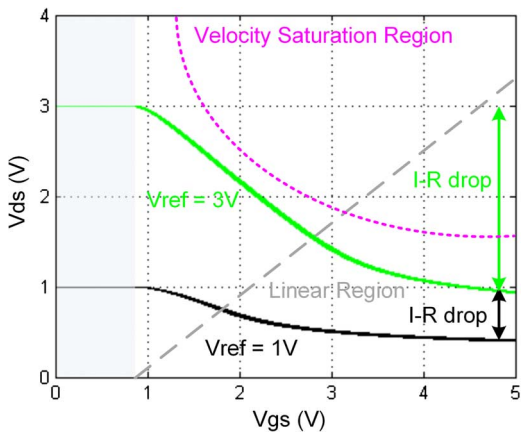


Fig. 4. Monte-Carlo simulation of the drain voltage variation dual parasitic resistance for the transistor in the linear and velocity saturation region.

in the readout transistor in each pixel are constant. The DC offset term $G_{CC}g_{m_{pxl}}V_{DC_{pxl}} + I_{DC_{CC}}$ can be removed by FPN cancellation techniques, thus, a linear mapping between $I_{readout}$ and the intensity can be achieved.

However, in the design of an image sensor array, the variation of $g_{m_{pxl}}$ and $V_{DC_{pxl}}$ between pixels must be taken into account which makes the cancellation of FPN very difficult. In addition, photon shot noise, reset noise, readout noise due to thermal and flicker noise, and FPN from parasitic mismatch due to routing differences, all have effects on the results. Thus, (9) can be further modified as

$$I_{rst} = G_{CC}\left[\left(g_{m_{pxl}}(V,x,y) + \Delta g_{m_{pxl}}(x,y)\right) \times \left(V_{DC_{pxl}} + \Delta V_{DC_{pxl}}(x,y)\right) + \bar{i}_{rst} + \bar{i}_{read,rst}\right] + I_{DC_{CC}} \quad (10)$$

and

$$I_{exp} = G_{CC}\left[\left(g_{m_{pxl}}(V,x,y) + \Delta g_{m_{pxl}}(x,y)\right) \left(\frac{Q_{photon}}{C_{pxl}(V)} + \frac{Q_{shot}}{C_{pxl}(V)} + i_{dark}\cdot t_{int} + V_{DC_{pxl}} + \Delta V_{DC_{pxl}}(x,y)\right) + \bar{i}_{rst} + \bar{i}_{read,int}\right] + I_{DC_{CC}} \quad (11)$$

where I_{rst} represents the current readout after the reset phase, while I_{exp} is the readout after exposure. $\bar{i}_{rst}$ and $\bar{i}_{read,rst}$ stand for the reset noise and the readout noise in the reset phase, respectively. Q_{shot}, i_{dark} and $\bar{i}_{read,int}$ represent the integrated shot noise, the dark current and the readout noise after the exposure phase, respectively.

There are two major sources of FPN: gain FPN and offset FPN [30]. According to (10) and (11) the gain FPN can be written as,

$$FPN_{gain} = G_{CC}\left(g_{m_{pxl}}(V,x,y) + \Delta g_{m_{pxl}}(x,y)\right) \quad (12)$$

Due to the transconductance variation, current mode imagers usually suffers from more serious FPN than voltage mode. The offset FPN is equal to

$$FPN_{offset} = FPN_{gain}\cdot \Delta V_{DC_{pxl}}(x,y) \quad (13)$$

where $\Delta V_{DC_{pxl}}$ mainly comes from the threshold variation ΔV_{TH} across the pixel array.

The widely used correlated double sampling (CDS) or delta-reset sampling subtracts the reset current from the captured signal, by doing so, the $\bar{i}_{rst}$ and part of the offset FPN can be cancelled. However, the gain FPN and shot noise can not be cancelled. In addition, the readout noise is increased.

The linearity of a current mode image sensor can be improved by reducing the FPN. Both FPN_{gain} and FPN_{offset} can be suppressed by reducing the variation of $g_{m_{pxl}}$ and G_{CC}. In addition, a gain calibration can further lower the FPN. Correspondingly, a higher signal-to-noise ratio (SNR) and a higher dynamic range (DR) can be achieved.

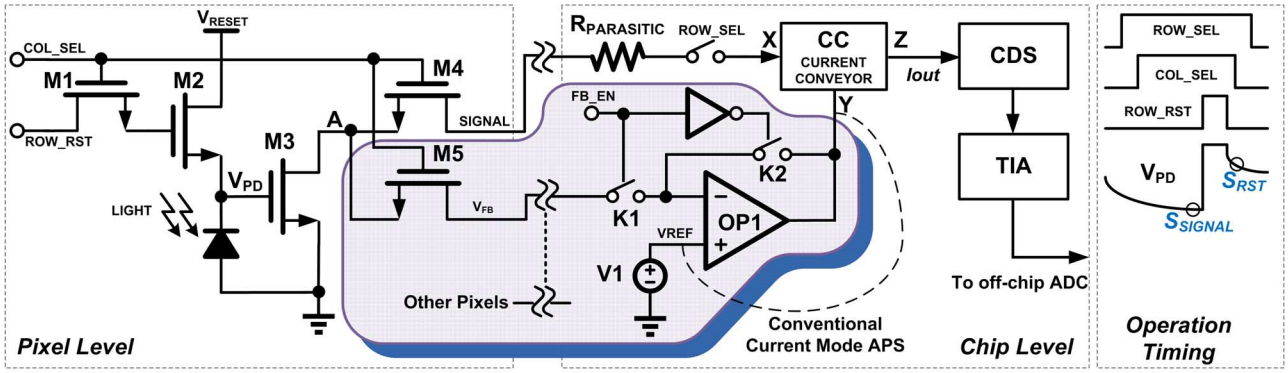
III. Proposed Architecture of the Current Mode Image Sensor

A. Pixel Structure

To address the nonlinearity and noise limitations of the current mode APS as illustrated in the previous section, an integrated linearity enhancement circuitry is developed as shown in Fig. 5(a). The proposed circuit includes a standard current mode APS, with a readout transistor M_1, and reset/select transistors M_2 and M_3. The shadowed region highlights the proposed linearity enhancement circuit. At the pixel level, a feedback switch M_5 is connected to node "A" which is employed to sense the V_{DS} voltage of the readout transistor M_1. At the chip level, in the readout circuit, a feedback amplifier and several switches are inserted.

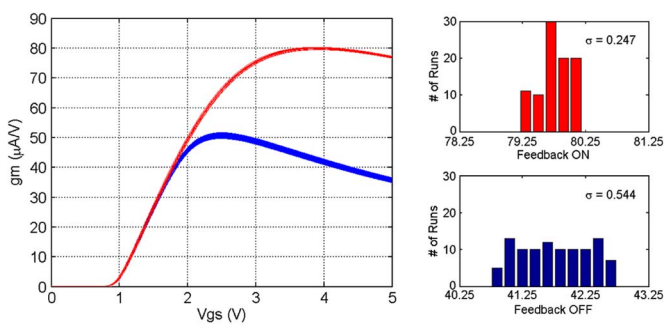
The proposed imager can operate in feedback mode or non-feedback mode, controlled by signal FB_EN. When FB_EN is low, the imager operates in non-feedback mode. OP_1 is configured as a unity gain buffer driving node "Y" to the voltage of V_{REF}. Since K_1 is open, the feedback voltage V_{FB} will not affect the operation. When FB_EN is high, K_1 is closed and K_2 is open. The APS works in feedback mode where a negative feedback loop, composed of the pixel, CC and OP_1 is formed. OP_1 drives node "Y" and consequently sets the voltage on node "A" through the CC. Since the negative input of OP_1 is a high impedance node, there is no current flowing through M_5, making the I-R drop along the databus from node "A" to the negative input of OP_1 negligible. The large open loop gain from OP_1 forces the voltage at node "A" to be the same as V_{REF}, which keeps the V_{DS} of M_1 to be the same for different pixels and for different output current levels.

In order to reduce the mismatches and channel length modulation of the readout transistors, a relative larger channel width and length should be used. However, that will increase the required drain voltage for velocity saturation, which is not applicable for a low voltage process. In addition, a larger transistor size occupies more silicon area, resulting in a reduction of the fill factor. In the proposed pixel, M_1 and M_4 are implemented with the smallest feature size ($\mathrm{W/L} = 0.9\ \mu\mathrm{m}/0.6\ \mu\mathrm{m}$) to achieve a higher fill factor and reduce the output current without sacrificing the performance. V_{DS} of M_1 is set to 1.3 V to limit the maximum current and bias the channel in the moderate velocity saturation region.



(a) (b)

Fig. 5. (A) APS operating in the current readout mode. The shadowed region illustrates the proposed feedback loop between the readout transistor and the CC for the purpose of linearity enhancement. (B) Simplified timing diagram of the control signals.



(a) (b)

Fig. 6. 100-run Monte-Carlo simulation of the transconductance with feedback ON(red)/OFF(blue). The standard deviation of the transconductance improves 54.6% by applying the proposed feedback circuit.

A 100-run Monte-Carlo simulation of the proposed feedback mechanism is performed, as illustrated in Fig. 6. Variations of the parasitic resistance on the signal path are set according to the extraction of the sensor array layout. By applying the proposed feedback loop, the transconductance of the readout transistor has a more flatten region. In addition, a 54.6% improvement of the standard deviations of the transconductances is achieved. According to the non-linearity and noise analysis in previous sections, the improvement of $g_{m_{pxl}}$ reduces the FPN, thus, improving the SNR and DR.

B. Readout Circuit

Fig. 7 illustrates the current conveyor (CC) circuit [29]. The CC circuit translates the voltage on "Y" to "X", and mirrors the current from the input branch "X" to the output branch "Z". Performance of the CC depends on how accurate the current can be conveyed from "X" to "Z" as well as the voltage translated from "Y" to "X".

To achieve high accuracy, a high output impedance at the output node "Z" is required which can be realized by cascode technique. The cascode structure also helps to maintain the same voltage between "X" and "Y". In this work, the CC incorporates a low voltage cascode structure to provide more head room making it suitable for low voltage application. The cascode bias voltage VBP and VBN are generated from replica biasing which can better track the PVT variations. For this design, all the NMOS mirrors are of the same size while M_3 is

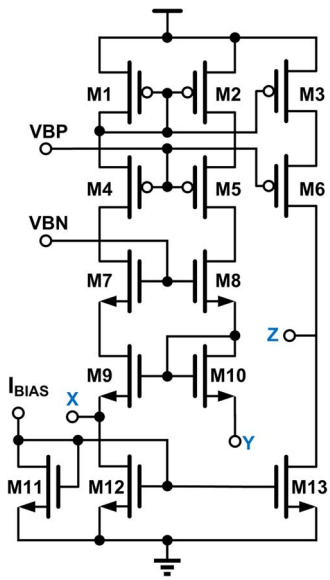


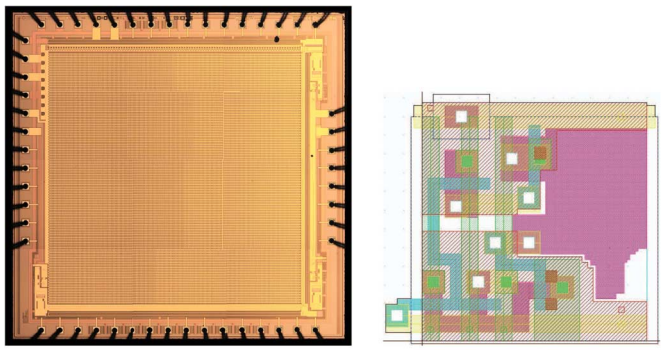
Fig. 7. High swing current conveyor employing low voltage cascode current mirror.

slightly wider than M_1 and M_2 which gives a current scaling ratio k defined by the ratio of their width. This will result in V_X=V_Y and

$$I_Z = kI_X + (k-1)I_{BIAS} \tag{14}$$

The second term in (14) is a fixed offset that can be cancelled by the CDS.

In the CC, the terminals "X" and "Y" are "virtually" connected when operating at low frequency. The parasitic capacitance on "X" will directly effect the pole of the output stage of the folded-cascode amplifier OP_1. In order to make the system stable under all circumstances, a single pole amplifier is employed. Since the parasitic capacitance generated on "X" will further pushes the output stage pole of the amplifier to a lower frequency, the feedback can be stable under any illumination condition. In addition, the poles generated from $M_{1,2,4,5,7,8}$ are designed to be 10 times higher than the one of the amplifier, which guarantees the pole of the amplifier will be the main pole of the circuit.



(a) (b)

Fig. 8. (A) Microphotography of the fabricated chip. (B) Layout of the pixel. The pitch size is 12 μm, with a fill factor of 31%.

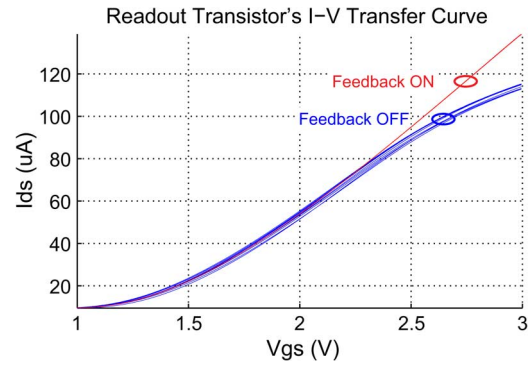
IV. Experimental Results

The image sensor consisting of an array of 100 × 200 pixels was fabricated using 0.5 μm 2P3M standard CMOS process and occupies an area of 3 mm × 3 mm. A microphotograph of the sensor array is shown in Fig. 8 as well as the layout of the pixel. Even with the additional feedback transistor in the 12 μm × 12 μm pixel, a fill factor is of about 31% is achieved.

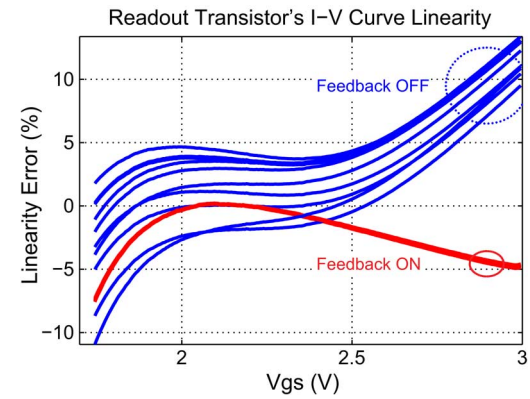
Fig. 9(a) compares the readout current of 10 different pixels while the proposed feedback loop is turned on and off, respectively. At small V_{GS}, all the output currents are almost the same because the I-R drop is not significant. When V_{GS} exceeds 2.2 V which biases the readout transistor in the linear region, the curves start to deviate in the feedback-off case: 1) The current is smaller for the same V_{GS} compared to the feedback-on value. This error is due to the large total parasitic resistance. 2) The current of different pixels shows large variations. This error is mainly caused by the mismatch of the switches. In contrast, for the feedback-on case, all 10 pixels show identical output current across the whole V_{GS} range proving that the proposed structure works well to cancel out the parasitic resistance.

The measured transconductance of the readout transistor is plotted in Fig. 10. For the designed structure, when V_{GS} is small, the g_m difference is small. As V_{GS} exceeds 2.2 V in the feedback-off case, the readout transistor enters the linear region and its g_m drops due to V_{DS} variation and mobility degradation. On the other hand, when the feedback is on, the transconductance g_m is relatively constant up to V_{GS} of 3 V, which confirms the simulation results. The linearity error, plotted in Fig. 9(b), is based on the linear fit of the I-V curve from $V_{GS} = 1.7$ V to 3 V which corresponds to the constant region of the g_m curve. The linearity error without feedback shows large variations due to the resistance difference. The standard deviation is 2.45% with feedback and 4.49% without feedback that corresponds to a 45% improvement, which also matches the Monte-Carlo simulation results.

An off-chip 12-bit analog to digital converter (ADC) is employed to digitize the output signal. The digitized pixel output after the reset phase with the proposed feedback loop off and on is illustrated in Fig. 11. By employing the proposed feedback loop, the mismatch between the reset value is greatly reduced. The standard deviation of the reset frame is 52.6 DN without the feedback, and 22.3 DN while the feedback is turned on. A significant improvement of 57.6% is achieved. It should be noted



(a)



(b)

Fig. 9. (A) Measured I-V transfer curve at 10 different pixels with feedback ON/OFF. (B) Measured I-V curve linearity error at 10 different pixels with feedback ON/OFF.

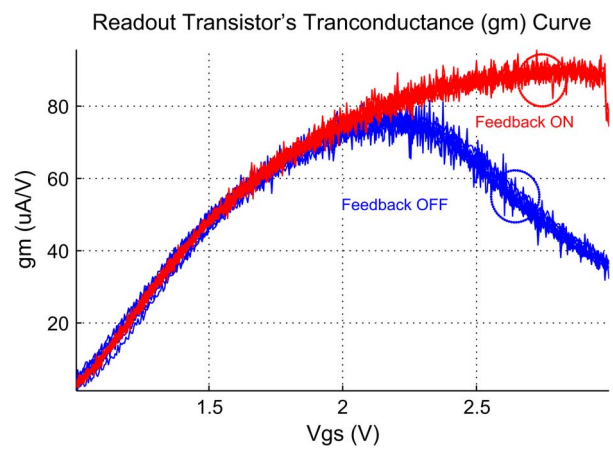


Fig. 10. Measured transconductance at 10 different pixels with feedback ON/OFF.

that a gradual change of reset noise level can be seen for the case without feedback, which is the result of drain voltage variation due to I-R drop across the array.

Fig. 12 further compares the standard deviation of the digitized pixel readout after exposure. The same diffused LED light source is applied with different flash times. The distribution of the pixel readouts without feedback is illustrated in blue bars while the red bars represent the case when feedback is turned on. The experimental results confirms the previous schematic simulation results.

Fig. 13 compares the measured photon transfer curve [28] under different conditions. At low light intensity, the noise level

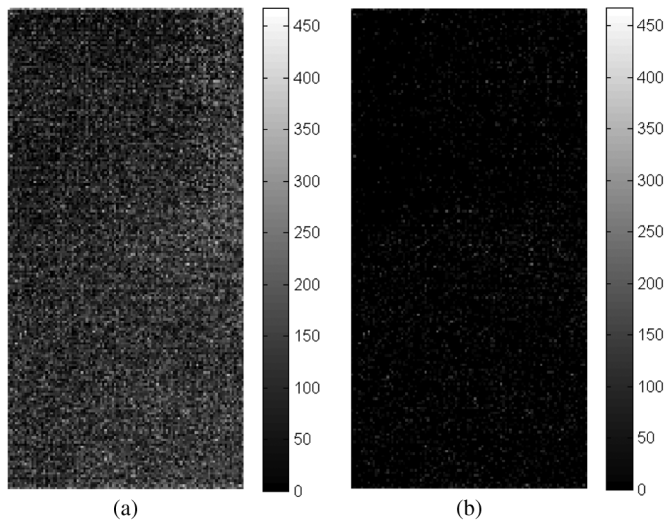


Fig. 11. Digital readout after reset. (A) with feedback off, the σ is 52.6 DN, and (B) with feedback on, the σ is 22.3 DN. An improvement of 57.6% is detected.

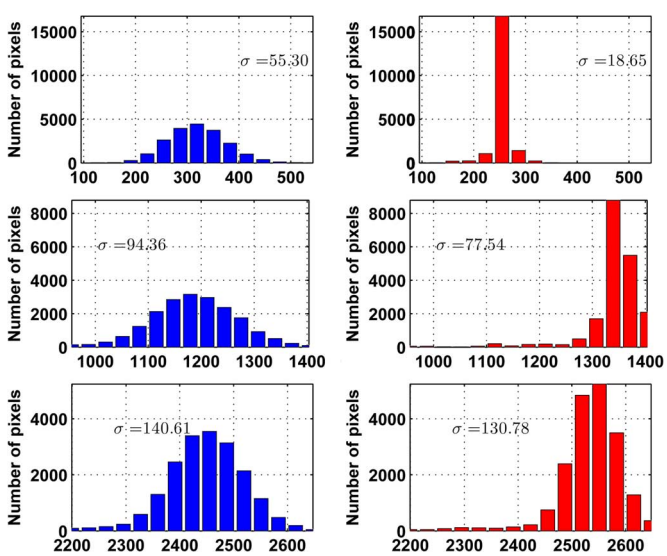


Fig. 12. Comparison on the digitized pixel output after a same exposure time while the feedback is turned (left) off and (right) on. The distribution of the readout value is presented in histogram. The standard derivation of the readout value is calculated and labeled on each figure.

for both feedback on and off are the same since the noise is dominated by read noise and photon shot noise. With feedback off, the noise is larger without CDS. With feedback on without CDS, the noise level is lower than the feedback off curve with CDS on. For FPN dominated region, the noise level at full well capacity point is reduced from 5.27% to 4.29%, since the transconductance variation is restrained and the linearity is improved, as analyzed in the previous sections. A FPN of 0.7% is measured while the feedback is turned on. A gain calibration is employed to further reduce the FPN. The gain factors of each pixel are extracted from uniform illumination samples near full well capacity. With gain calibration, the noise in the FPN dominated region gets significant improvements, and the noise level at full well capacity point is reduced to 2.08%. Sample images are shown in Fig. 14. The image quality is visually improved.

Table I compares the proposed work with previous current mode image sensors reported in the literature. The raw FPN, which is the raw measured noise level without any post data processing, is reduced while the other specification is comparable to the reported works.

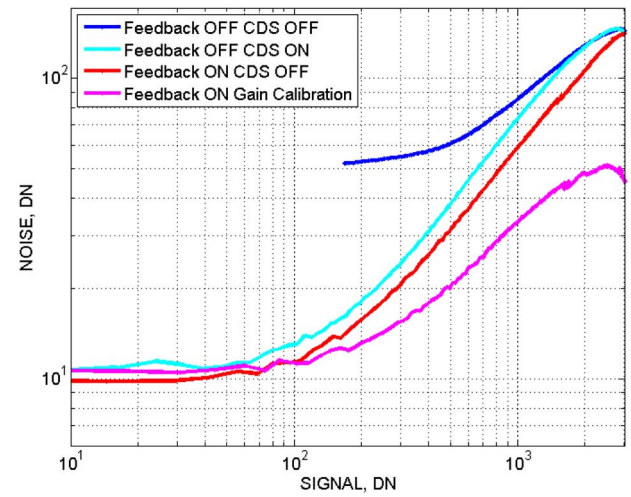


Fig. 13. Photon transfer curve measured for the entire frame with feedback ON/OFF, with CDS ON/OFF and additional gain calibration.

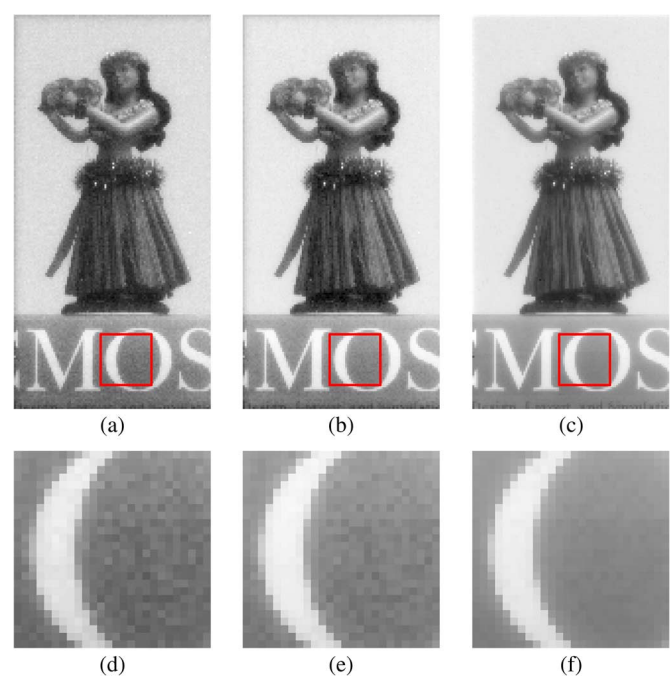


Fig. 14. Sample image captured by the proposed current mode APS with (A) feedback loop turned off, (B) feedback loop turned on, and (C) feedback loop turned on and a gain calibration is applied. While (D-F) shows zoom-in view.

TABLE I
COMPARISON OF CURRENT MODE IMAGE SENSOR IN LITERATURE

	This work	[24]	[23]	[34]
Process	0.5um	0.5um	0.5um	0.35um
Array size	200x100	110x200	50x128	128x96
Frame rate	30fps	30fps	–	9.6fps
Supply voltage	5V	5V	5V	1.35V
Pitch (um^2)	12x12	12x12	18x18	21x21
Fill Factor	31%	31.25%	44%	39%
Dark current	1.2fA	1.18fA	2.8fA	–
FPN(raw)	0.7%	3.8%	2.5%	>1%
Dynamic range	49.6dB	46.6dB	–	60dB

V. Conclusion

In this paper, a current-mode image sensor with an integrated linearity improvement circuit is demonstrated. The proposed feedback loop enables the readout transistor operating at a relative constant V_{DS} independent of the parasitic interconnection and switch resistance. According to the theoretical analysis, mismatch and parasitic resistance from switches and routings can be compensated by employing the feedback loop. The readout transistor can operate with a lower V_{DS} voltage which is critical for low power and low voltage process. Experimental results illustrate improved linearity and linear working range. Although the proposed feedback loop is shown to operate in velocity saturated region, the same topology can be applied to a sensor array with readout transistors biased in the linear region as well, where V_{DS} is a key factor in the output current.

Overall, the proposed modification to the current mode sensor has improved the performance significantly, thus making it an alternative option to a voltage mode imagers for cases where current mode is more suitable, e.g. focal plane image processing, and/or when online arithmetic processing is required. In this paper, a thorough analysis of the FPN has been performed as a way to reduce its effect.

Acknowledgment

The authors would like to thank MOSIS for the chip fabrication and Dr. Z. Yang for the useful discussions.

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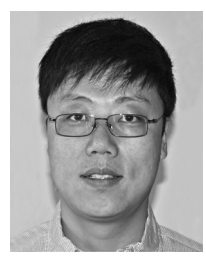

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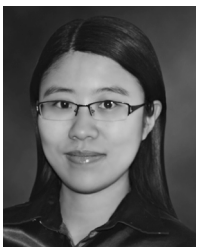

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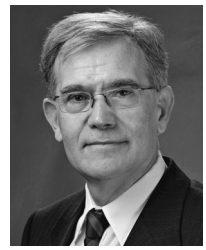

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